CLAIMS

1. A display device comprising:

a plurality of discharge cells;

a clock signal generator that generates a clock signal;

a serial data generator that generates serial data according to an image to be displayed;

a test signal generator that generates a test signal;

a data driver that selectively applies a drive pulse to said plurality of discharge cells based on the serial data generated by said serial data generator in synchronization with said clock signal in a write period for selecting the discharge cell to be lighted;

a latch failure detector that detects the presence/absence of a latch failure in said data driver based on the test signal generated by the test signal generator in a period other than said write period; and

a phase adjusting device that when the latch failure is detected by said latch failure detector, adjusts the phase of the clock signal provided from said clock signal generator to said data driver, based on the phase of the clock signal in which the latch failure is detected.

2. The display device according to claim 1,

wherein said data driver includes a plurality of data

driver units;

said latch failure detector includes a plurality of latch failure detecting circuits that detect the presence/absence of the latch failure by the respective data driver units based on the test signal outputted from said test signal generator; and

when the latch failure is detected in at least one of said plurality of latch failure detecting circuits, said phase adjusting device adjusts the phase of the clock signal provided to said plurality of data driver units from said clock signal generator.

3. The display device according to claim 2,

wherein said plurality of latch failure detecting circuit each have an open drain output; and

said phase adjusting device receives the open drain outputs of said plurality of latch failure detecting circuits via wired-OR connection.

4. The display device according to claim 1, wherein said test signal is an alternating pulse signal that is inverted every period of said clock signal.

5. The display device according to claim 1, wherein said phase adjusting device adjusts the phase of the clock signal at predetermined intervals.

6. The display device according to claim 1, wherein said phase adjusting device adjusts the phase of the clock signal at intervals of a plurality of fields.

7. The display device according to claim 1, wherein said phase adjustment period includes a plurality of adjustment periods; and

said phase adjusting device continues, when the adjustment of said clock signal has not finished in one adjustment period, the phase adjustment of said clock signal from the beginning of the next adjustment period.

8. The display device according to claim 4, wherein said latch failure detector generates a latch failure detection signal indicating the presence/absence of the latch failure, based on an exclusive logical sum of a first test signal obtained by delaying said test signal by one period of said clock and a second test signal obtained by delaying said test signal by two periods of said clock.

9. The display device according to claim 8, wherein said latch failure detector generates a plurality of latch failure detection signals obtained by sequentially delaying said latch failure detection signal by a predetermined delay amount to

generate a logical product of said plurality of latch failure detection signals.

10. The display device according to claim 1, wherein said latch failure detector includes a holding circuit that holds a detection result of the latch failure until a reset signal is inputted.

11. The display device according to claim 10, wherein said latch failure detector further includes a reset signal generating circuit that generates said reset signal based on the detection result of the latch failure.

12. The display device according to claim 11, wherein said reset signal generating circuit includes a delay circuit that delays the detection result of the latch failure.

13. The display device according to claim 1,

wherein said phase adjusting device includes:

a ring buffer including a plurality of delay elements that sequentially delay said clock signal by a predetermined delay amount; and

a selector that selectively outputs a plurality of clock signals outputted from said plurality of delay elements of said ring buffer.

14. The display device according to claim 1,

wherein said phase adjusting device includes:

a plurality of delay circuits each having a different number of delay amounts; and

a connecting circuit that selects one or more of said plurality of delay circuits so as to constitute a series-connecting circuit by the selected one or more of said plurality of delay circuits and provides said clock signal to said series-connecting circuit.

15. The display device according to claim 1, wherein said phase adjusting device finishes the adjustment of the phase of said clock signal by the time said clock signal is delayed by two periods.

16. The display device according to claim 1, wherein the phase adjusting device is operable to detect that the phase of the adjusted clock signal is the optimal phase and finish the adjustment of the phase of said clock signal when it is detected that the phase of the clock signal is the optimal phase.

17. The display device according to claim 1, further comprising a first storage device that stores the phase of the clock signal adjusted by said phase adjusting device as the

optimal phase,

wherein said phase adjusting device adjusts the phase of said clock signal to said optimal phase stored in said first storage device in the write period after said optimal phase is stored by said first storage device.

18. The display device according to claim 17, wherein said phase adjusting device adjusts the phase of said clock signal to the phase stored in advance in said first storage device when the adjustment of said clock signal has not finished in said adjustment period.

19. The display device according to claim 17, wherein said phase adjusting device varies the phase of said clock signal to detect a range of phase where no latch failure occurs and when the detected range is larger than a predetermined threshold, stores, in said first storage device, a phase in the center of said detected range of phase as said optimal phase.

20. The display device according to claim 17, wherein said phase adjusting device adjusts the relative phase of the clock signal with respect to said serial data so that said adjusted clock signal is outputted to the data driver just as a start portion of said serial data is outputted to said data driver.

21. The display device according to claim 20, wherein, said phase adjusting device adjusts the phase of said serial data so that the phase of the start portion of the serial data outputted to said data driver and the phase of the start portion of the clock signal outputted to said data driver substantially coincide with each other when it is detected that the phase of said clock signal is the optimal phase.

22. The display device according to claim 21, further comprising a second storage device that stores the phase of said serial data adjusted by said phase adjusting device as an optimal phase,

wherein said phase adjusting device adjusts the phase of said serial data to said optimal phase stored in said second storage device in the write period after said optimal phase is detected by said second storage device.

23. The display device according to claim 22, wherein said phase adjusting device adjusts the phase of said clock signal to the optimal phase stored in said first storage device last time and adjusts the phase of said serial data to the optimal phase stored in said second storage device last time when the optimal phase of said clock signal or the optimal phase of said serial data is not detected.

24. The display device according to claim 1, wherein said adjustment period is set to a sustain period during which light emitting of the discharge cell selected in said write period is sustained.